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MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA

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Comprehensive validation solution for silicon IP & library

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Agenda

- Motivation
- Main idea: ST CAD IP signoff solution
- Example checks
- Solution scalability
- Results
- Summary

Motivation: IP* CAD signoff is complex & time consuming

- With evolving EDAs, IP CAD Views are increasing exponentially
- IP CAD view generation is the last milestone in IP development cycle
- IP CAD view quality is crucial for accurate & timely SoC signoff

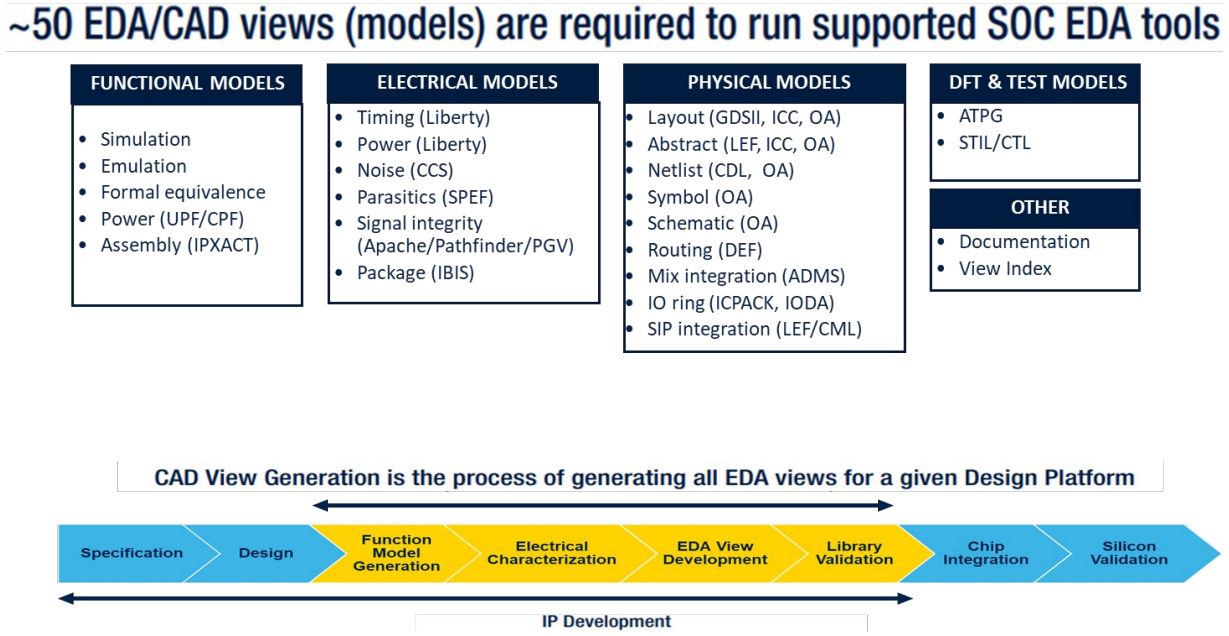
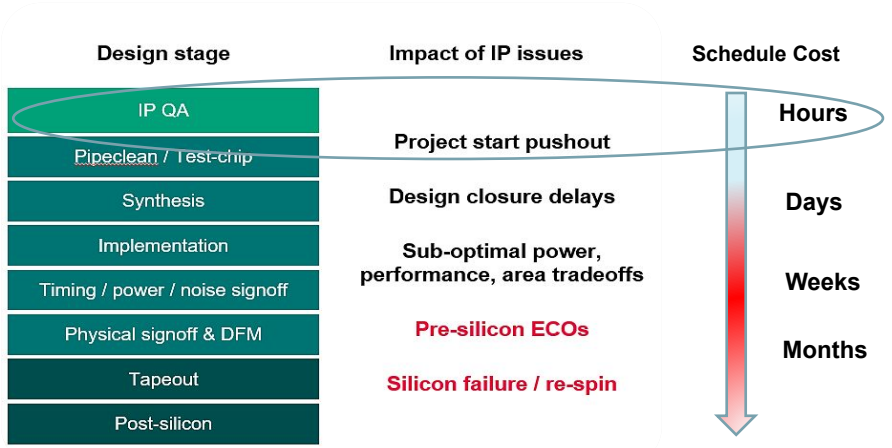


Fig.1 : IP Development cycle & CAD views

** IP : Analog Macro, Digital Macro, IO, Memory, Standard Cells.*

Motivation: need for robust IP validation solution

- Inefficient IP validation leads schedule cost of discovering late issues in SoC



- Need robust QA matrices for IP validation
  - Tool-agnostic IP usability
  - Consistent encapsulation of IP information
  - Performance consistent with IP specification

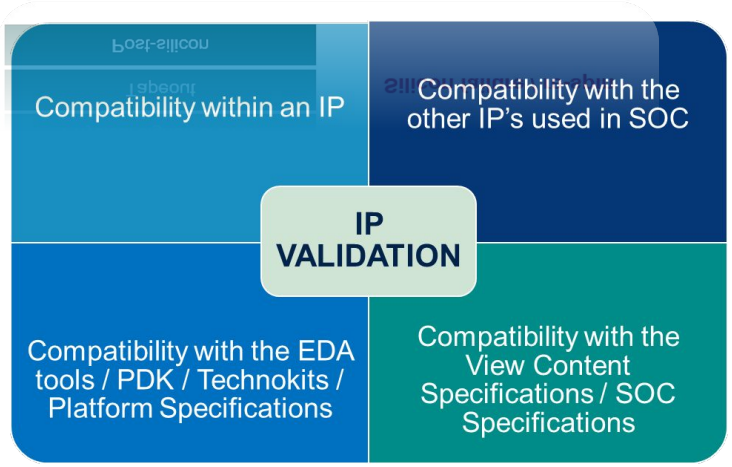


Fig.2: IP validation metrics

Main idea: IP CAD validation framework

- Identifying IP validation **QA metrics** and categorizing
- Defining set of checks per **view/across views** for various metrics

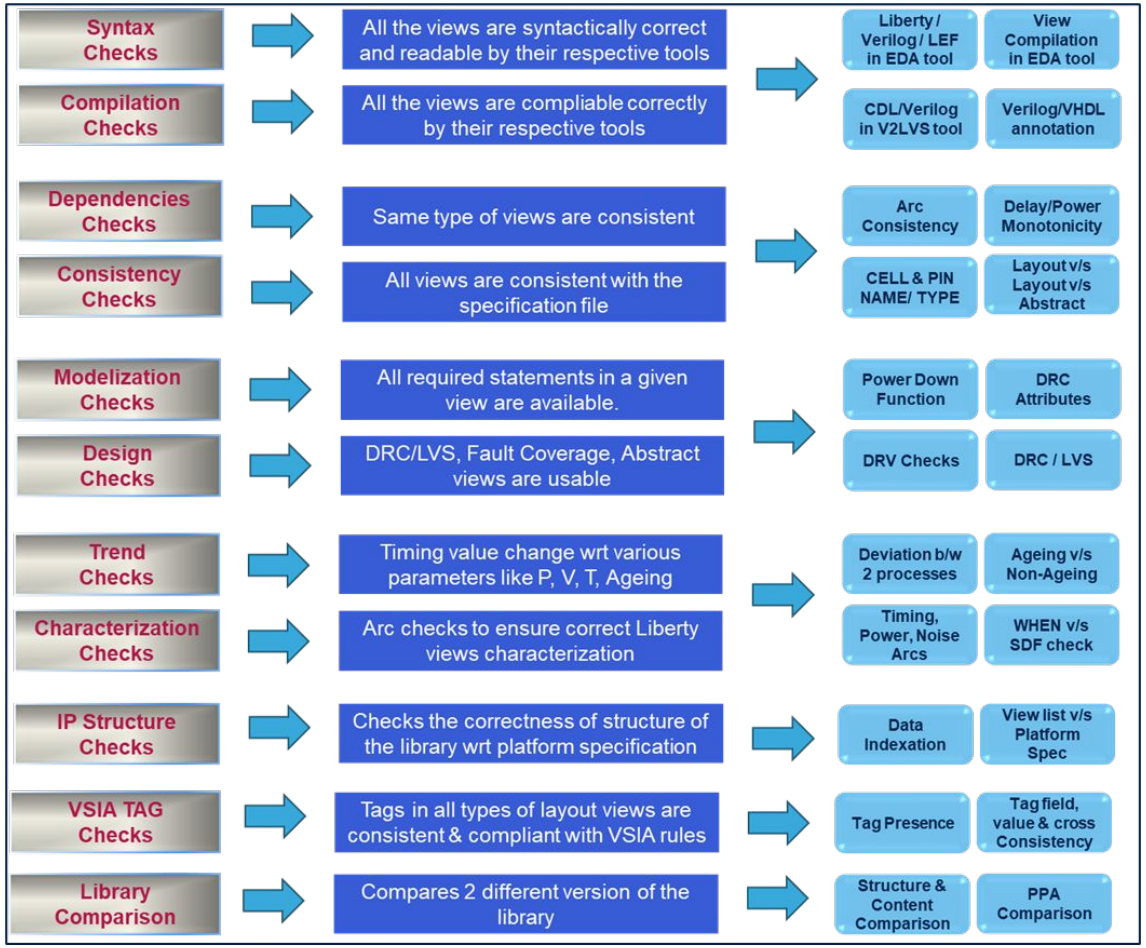


Fig. 3: Different checks need to signoff IP at CAD level (few examples...)

Main idea: IP validation solution using ST CAD infrastructure

- ST's in-house solution is designed
  - around **Solido Crosscheck**
  - with robust **API interface**

- Solution addresses:
  - Validation need for target IPs
  - Ensures compatibility among various IP components
  - Supports non-ST techno's and IPs

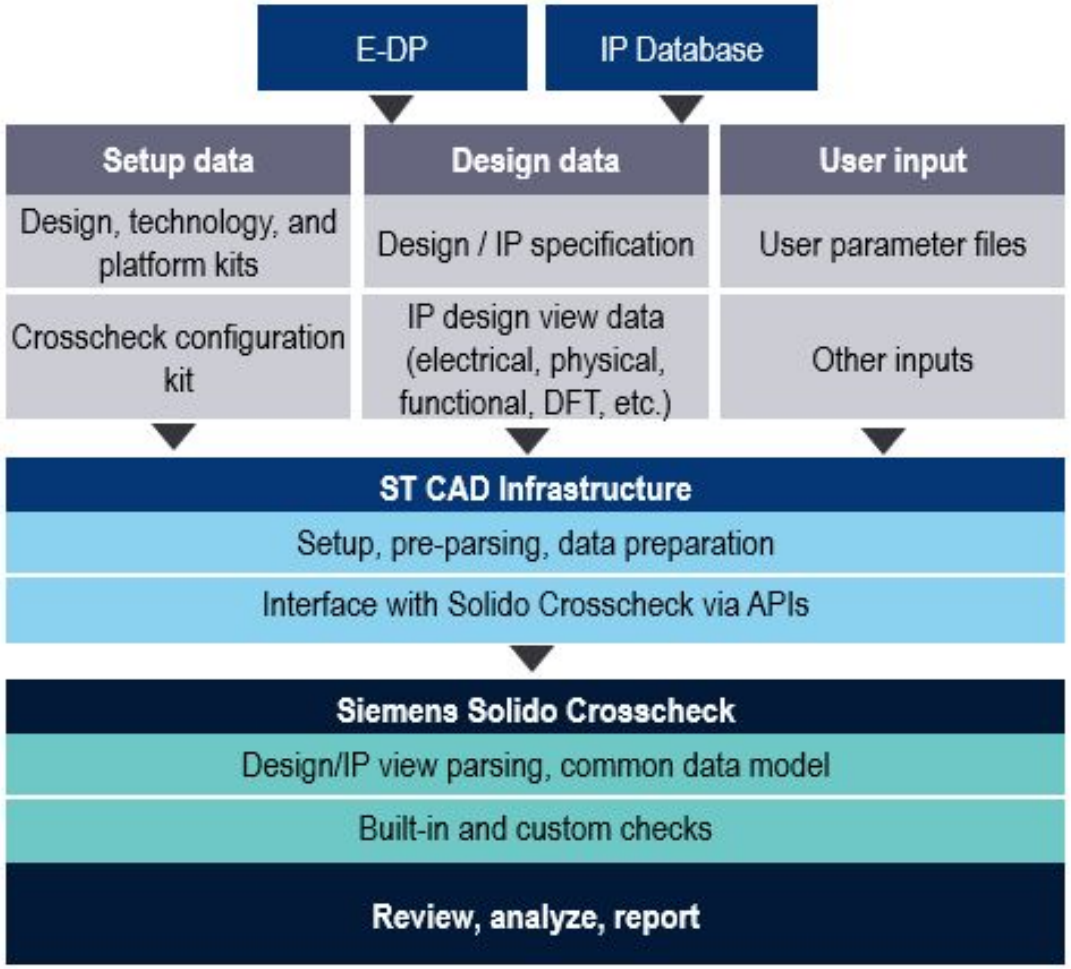


Fig. 4: ST in-house IP CAD validation solution

Example checks performed: cross-view consistency

- Cells/ pins/ nets may be inconsistent

TBs of data size to be checked

- Core Libs with ~1000 cells
- Macros with ~ 100's of ports/pins
- Advance node ~ 50-100 process corners

- Potential issues at SoC implementation
  - Cell/Pin name mismatches, missing cells/pins… and area mismatches

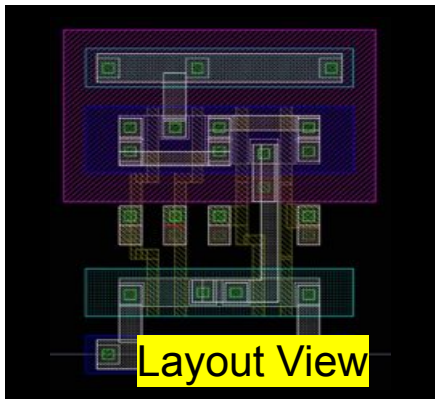
```
MACRO ADVX2
  CLASS CORE ;
  ORIGIN 0 0 ;
  ...
  SIZE 20.0 BY 25.0 ;

SITE CORE ;
PIN D_in
  DIRECTION INPUT ;
  PORT
    LAYER M1 ;
      RECT 0.1 0.1 0.1 0.1
    END
END D_in
```

LEF View

```
module ADVX_2 (
  D_in,
  ResetA, …,
  CX,
  VX);
  input D_in,
  input ResetA,
  …
  output CX,
  output VX
   …
endmodule
```

Verilog View



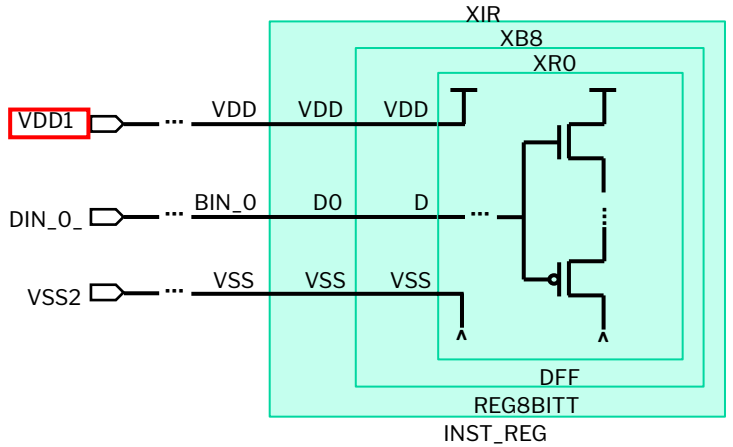

```
cell (ADVX2) {
  cell_footprint: ADV;
  area: 30;
  cell_leakage_power: 0.1;
  pin (DIN) {
    direction : input;
    capacitance: 0.05;
    …
    /* .lib table data */
  }
}
```

Liberty View

Fig. 5: Cross-View inconsistencies

Example checks performed: power domain mismatch between Spice CDL and Liberty (UPF)

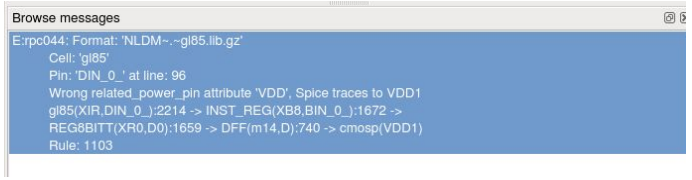
- Spice CDL vs Liberty (UPF) mismatch
  - Incorrect related power/ground pins
  - Incorrect power-down conditions
- Issues during chip-level design closure
  - Incorrect power domain associated to signal pins
  - LVS issues at chip level



in circuit

```
pin(DIN_0)
{
  related_power_pin: VDD2;
  related_ground_pin: VSS2;
  ...}
```

in liberty

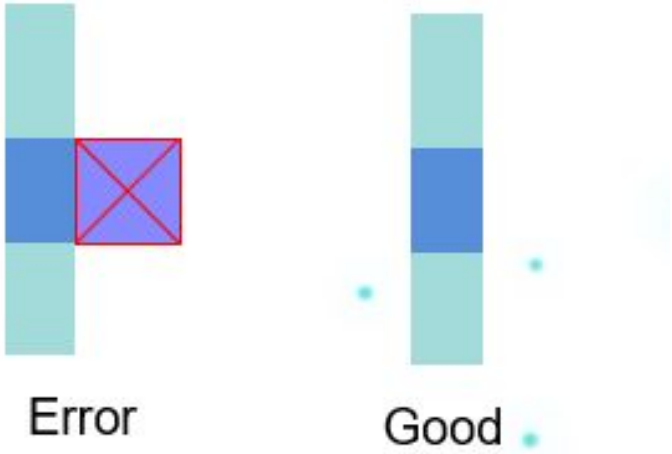


Error in validation solution

Fig. 6: Power domain mismatch

Example checks performed: abstract vs layout checks

- Inconsistency between LEF and GDS
  - Checks if abstract layer shapes cover all layout shapes
  - Shape coordinate differences are highlighted graphically



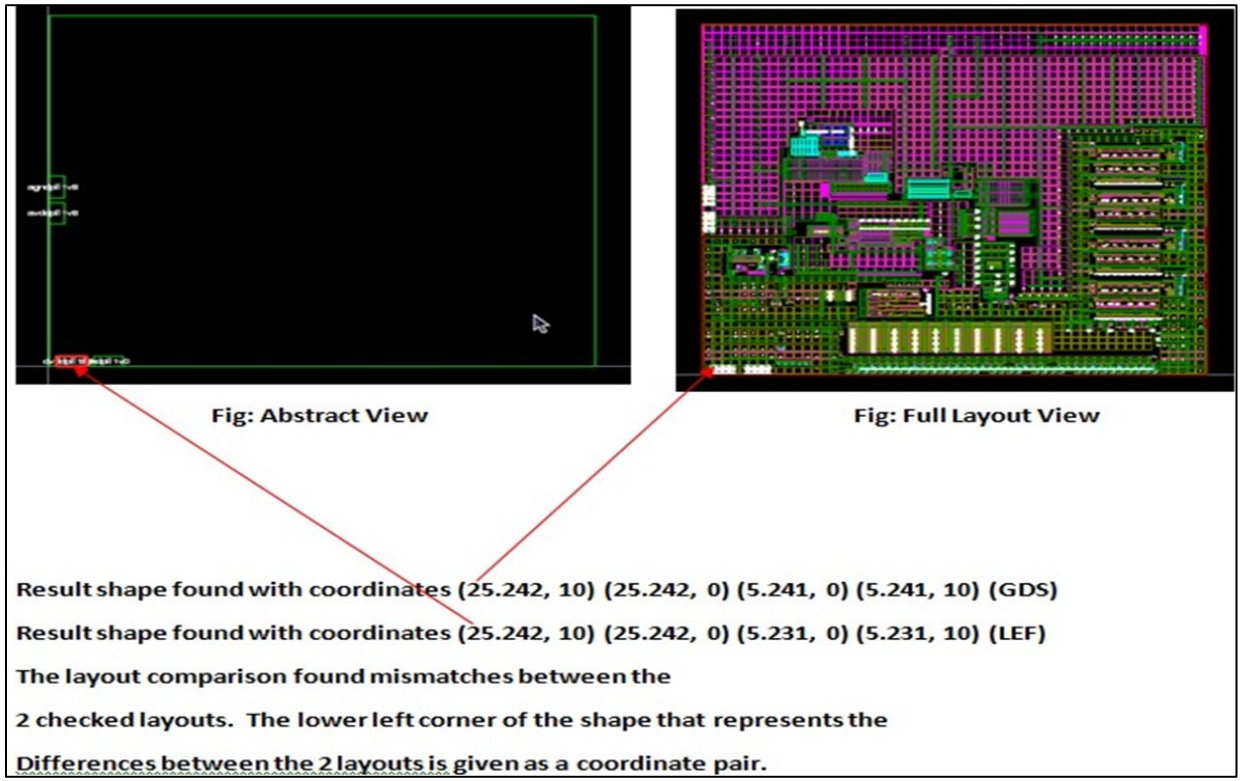
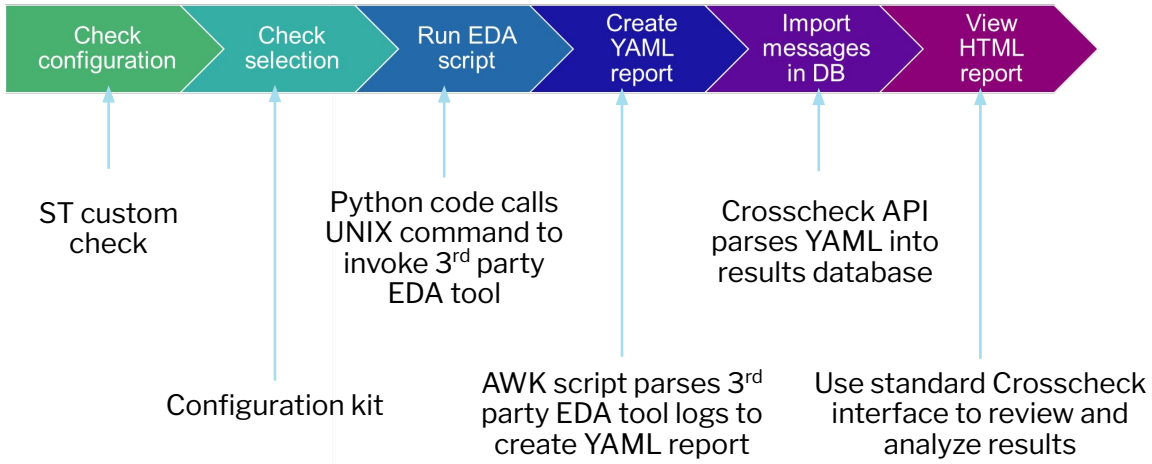


Fig. 7: Layout vs abstract check

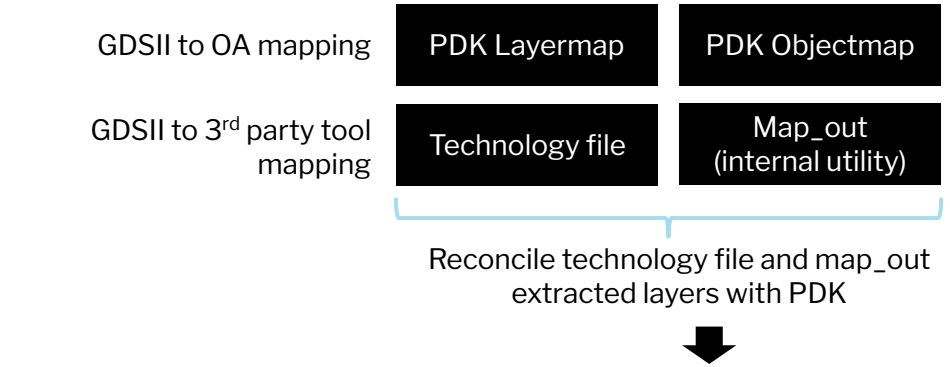
Example of solution scalability: integration of 3rd party EDA tools

Example 1: Integration of 3rd Party EDA Tools



Results: Repeatable, scalable, and automated process incorporating results from 3rd party tools into consolidated QA dashboard

Example 2: Technology Files Pre-parsing



Output: Correctly mapped layers, consolidated from PDK, GDSII, technology file and internal map_out tool

Benefit: Days of engineering time savings per technology / design iteration

```
layer definitions:
    layers:
        AP_LVSNC:
            Third Party Tool:
            - 245 151
            OpenAccess:
            - AP LVSNC
            gdsII:
            - 245 151
        AP_SRconnect:
            Third Party Tool:
            - 218 226
            OpenAccess:
            - AP SRconnect
            gdsII:
            - 218 226
        AP_abstract:
            OpenAccess:
            - AP drawing AP fill
```

Integrated process for launch -> execute -> review results

Automated physical layer extraction and mapping

Result: IP CAD signoff solution impact on CAD quality (1/2)

Category	Feature	Gain/Result
Efficiency	Setup, User Interface, Reporting & Debug	• **85% reduction in manual effort per delivery vs** native tool
	Performance	• **70% improvement in IP CAD signoff cycle time** vs previous
Quality	IP coverage	• **5 IP types** (macros, memory, IO and standard cells)
	Techno coverage	
	Check coverage	• **~53 techno's** (ranging from 130nm to 7nm) • **~175 Checks** enabled for all IP types
	View coverage	• **~50 CAD Views** enabling SoCs.
Scalability	Configurability & parameterization	• **66% saving of effort for tool development** & support
	Check Integration	• ST Custom checks, EDA checks .. in same framework • Convergence of checks (**5+ ST internal tools**) under one

Result: IP CAD signoff solution impact on CAD quality (2/2)

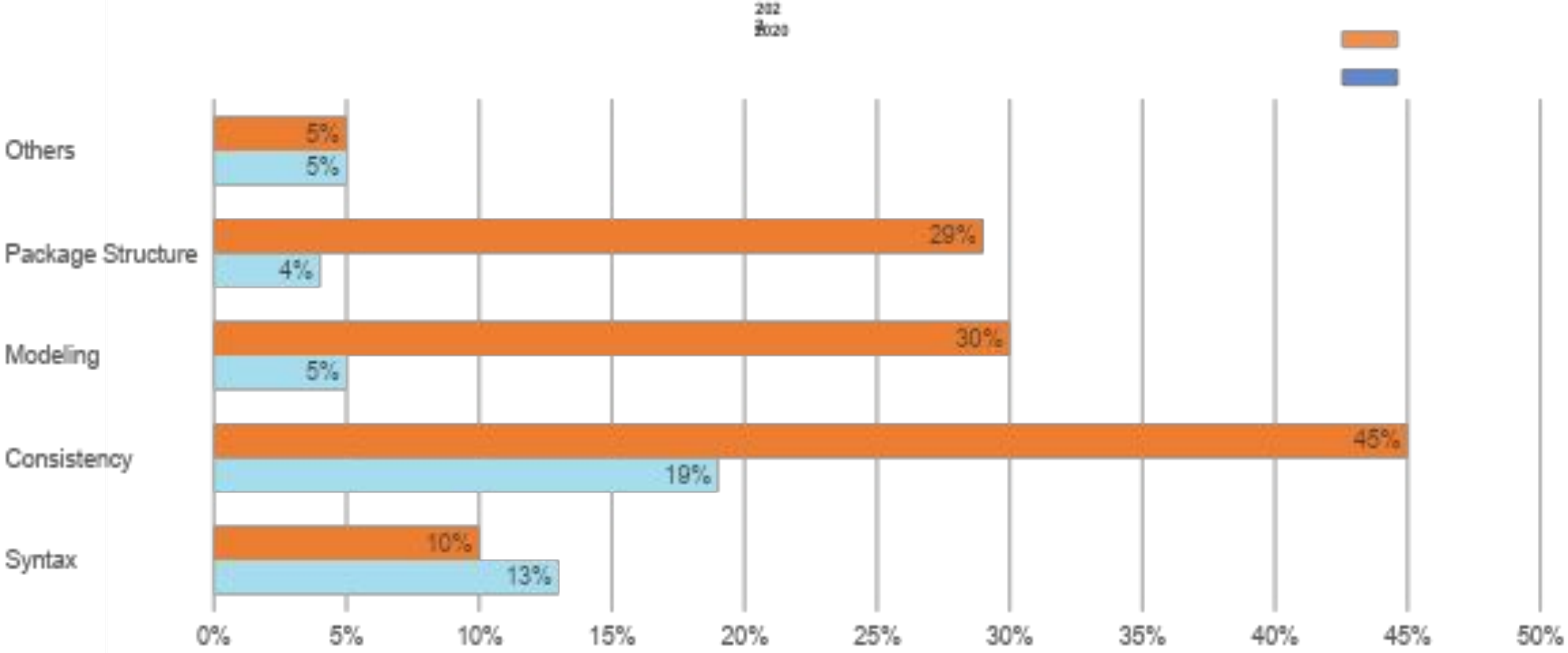


Fig.9: Progress over 2 yrs. in catching diverse types of issues using crosscheck solution

Summary

- Design IP data **has multiple CAD views and formats**

- **Robust IP QA is a must** for silicon quality and shorter SoC production schedule

- **85%** reduction in manual effort per IP delivery
- **66%** reduction in effort for validation tool development
- **30%** more issues detection (modeling, syntax, consistency, structure…)

- **Benchmarked** IP validation solution with industry standards (built-in checks…)

Single, integrated and homogeneous solution

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Thank You